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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/652,714	08/31/2000	Vishnu K. Agarwal	98-0616.09	3982

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EXAMINER

DIAZ, JOSE R

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 11/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/652,714

Applicant(s)

AGARWAL, VISHNU K.

Examiner

José R Díaz

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 37-39, 76-80 and 82-99 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 76-80 and 90-94 is/are allowed.
- 6) ☒ Claim(s) 37-39, 82-89 and 95-99 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 18, 19, 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

➤ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

➤ Claims 37-39, 82-89 and 95-99 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al. (US Patent No. 5,438,012) in view of Lee (US Patent No. 5,846,859).

Regarding claims 37 and 82, Kamiyama et al. teach a conventional method for fabricating a capacitor (see Figs. 4A-4D and 5-6) comprising the steps of: depositing a first conductive (3) (see Fig. 4A), incorporating an oxygen-free material (24) directly into said first conductive (see col. 4, lines 3-7), depositing a second conductive layer (6) (see Fig. 4D). However, Kamiyama et al. do not teach the step of exposing the second conductive layer to a thermal process, wherein said exposing step comprises: depositing an insulator over the second conductive layer and flowing said insulator. Lee teaches that is very well known in the art to form an insulator layer of BPSG on the upper electrode and then, flowing said insulator layer (see col. 1, lines 30-43). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kamiyama et al. to include the steps of depositing an insulator over the second conductive layer and flowing said insulator. The

ordinary artisan would have been motivated to modify Kamiyama et al. in the manner described above for at least the purpose of passivating the semiconductor device.

Regarding claims 38, 84, 88 and 98, Kamiyama et al. do not teach forming a trench capacitor. Lee teaches that it is well known in the art to form a trench capacitor to achieve DRAM with larger capacitance values without increasing the area these cells occupy on the chip (see col. 1, lines 10-45). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kamiyama et al. to include the steps of depositing a plug so that a trench capacitor is formed. The ordinary artisan would have been motivated to modify Kamiyama et al. in the manner described above for at least the purpose of increasing the capacitance values of the cells without increasing the area these cells occupy on the chip surface.

Regarding claims 39, 85, 89 and 99, Kamiyama et al. teach that the second conductive can be formed by an alloy process (see col. 4, lines 21-27).

Regarding claims 86-87 and 95-96, Kamiyama et al. teach a conventional method for fabricating a capacitor (see Figs. 4A-4D and 5-6) comprising the steps of: depositing a first conductive (3) (see Fig. 4A), incorporating HCl and then, NH_3 directly into the first conductive to passivate the surface of the first conductive layer to reduce the ability of the first conductive layer to associate with oxygen directly into said first conductive (see col. 3, lines 22-24 and col. 4, lines 3-7), depositing a second conductive layer (6) (see Fig. 4D). However, Kamiyama et al. do not teach the step of exposing the second conductive layer to a thermal process, wherein said exposing step comprises: depositing an insulator over the second conductive layer and flowing said

insulator. Lee teaches that is very well known in the art to form an insulator layer of BPSG on the upper electrode and then, flowing said insulator layer (see col. 1, lines 30-43), Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Kamiyama et al. to include the steps of depositing an insulator over the second conductive layer and flowing said insulator. The ordinary artisan would have been motivated to modify Kamiyama et al. in the manner described above for at least the purpose of passivating the semiconductor device.

Regarding claims 83 and 97, Official Notice is taken with respect to the limitation regarding the use of copper as a material for forming the second conductive layer since it is well known in the art that copper is a conventional material used in the semiconductor technology. For example, see layer 48 in Figures 7-8 of Applicant's disclosure, wherein Applicant clearly acknowledges the use of copper (48) as the second conductive layer of a capacitor to allow electrical communication with other semiconductor devices.

Allowable Subject Matter

- Claims 76-80 and 90-94 are allowed.

Response to Arguments

- Applicant's arguments with respect to claims 37-39, 82-89 and 95-99 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

➤ Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on September 24, 2002 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for

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the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
November 26, 2002

A handwritten signature in black ink, appearing to be 'JRD', is written over a faint, illegible stamp.